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WHITHAM, CURTIS & CHRISTOFFERSON & COOK, P.C.
11491 SUNSET HILLS ROAD
SUITE 340
RESTON, VA 20190

EXAMINER	
MOORE, IAN N	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/603,749	SCHRADER ET AL.	
	Examiner	Art Unit	
	IAN N. MOORE	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Claims 1, 6, 8, 17 and 18 are amended.

2. Claim objections, on claims 6-12 are withdrawn since they are being amended accordingly.

3. Claims 1-18 are rejected by the new ground(s) of rejection necessitated by the amendment.

Response to Arguments

4. Applicant's arguments, see pages 6-7 filed 6-27-08, with respect to the specification have been fully considered and are persuasive. The objection of the specification has been withdrawn.

5. Applicant's arguments, see pages 7-8, filed 6-27-08, with respect to 35 U.S.C, 112, first paragraph rejection of claims 13 and 14 have been fully considered and are persuasive (also in view of declaration under 37 CFR 1.132 filed on 2/1/08). The rejection under 35 U.S.C, 112, first paragraph of claims 13 and 14 has been withdrawn.

6. Applicant's arguments, under 35 U.S.C. 102 and 103 rejections, with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claims 1-18, the applicant argued that, "…Zahn …**PCI stands for Peripheral Component Interconnect**...video processing...This is not the same thing as time-synchronous data….Zahn video signal 50…data packets, so call frames 100…This data is clearly not time-synchronous….MPEG is a video encoding scheme… "Zahn does not disclose transmission of time-synchronous data and certainly does not disclose transmission of data using

a network of any type… This process is not real time….the point here is that the claimed invention is not a NLE system of Zahn type…Mr. Funaya notes that Zhan is directed to non-liner video editing which, by definition, is not time-synchronous transmission over a network… DSP load sharing scheme of Sastry is not the same or analogous to the claimed invention…Mr. Funaya notes again the claim 1..Zahn does not transmit any data but operates on a single machine…as to claim 2, Mr. Funaya notes that…Zahn does not change the parameters of a video editing unit after setup…as to claim 3, but Zahn switches before setup since the timing problems of component setup time do not matter for video editing…Sastry do not cover the problem of **setup time** at all…" in page 8-13.

In response to applicant's argument, the examiner respectfully disagrees with the argument above.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **PCI, MPEG, HDTV, NLE system, setup time**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Thus, it is arguing on the specific limitation set forth above, which are not being recited in the broad claim is irrelevant. In particular, applicant repeatedly arguing on PCI and its location, yet **none of the claimed invention limitation in the broad claim recites it**. Thus, Zahn disclosing or not disclosing, PCI and any of specific structure of any kind, has nothing to do with the claimed invention recited in the claim.

In response to argument on "time-synchronous multi-media" data, it is noted that applicant repeatedly arguing that Zahn **video data frame signal 50 (see FIG. 3)** is not the same as **"time-synchronous multi-media" data**.

In fact, applicant appear to confuse between the term "video" data signal encoded by MPEG or HDTV and term "synchronous multi-media" data. As one skilled in the ordinary art would clearly know that a **"video" signal data is synchronous multi-media signal data** since it is being transmitted at real time, and the user is able to view the video time synchronously at real time, otherwise, it would be just "a picture or image". To support this well known fact, examiner has attached Newton' Telecom Dictionary which define the term "video" as "motion picture" and "multi-media".

In response to the applicant argument that "time-synchronous multi-media data" does not equate to a video/audio data such as "MPEG or HDTV", first, "time-synchronous data" is a broad term, and every data that are processed "time-synchronously" is asserted as time-synchronous data. Second, **applicant own specification recites** "audio/video" senders in background of the invention as **well known in practice**. In particular, the specification page 1, para. 3 recite as follows:

> Mechanisms for the transmission **of time-synchronous data** are **well-known in practice** and are very well suited for the transmission of multimedia purposes, like **video** conferences, **telephone calls** and others. [Emphasis added]

Thus, applicant augments and the specification does not agree. The applicant owns specification recites this fact as "well-known in a practice". Moreover, one skilled in the art would clearly see that time-synchronous multi-media video data is being represented by MPEG

or HDTV data signal. Thus, arguing MPEG and HDTV data signals are not "time-synchronous" data is clearly an error.

Even applicant admits this fact, in this remark, by stating in page 9, lines 19-20 as set forth below.

"**Zhan describes implement** MPEG video encoding on **video frames** that have resolution meeting the HDTV definition".

In particular, Zhan disclose receiving time-synchronous multi-media data **(see FIG. 1, 2, receiving real time/synchronous video/multi-media signal 50 (see FIG. 3) utilizing MPEG or HDTV at apparatus 1; page 4, paragraph 3-8; see page 9, last paragraph)**.

In repose to applicant argument on the amended limitations on claims 1-18, identical to applicant claimed invention, the combined system of Zahn and Sastry discloses operating the video data and transmitting the video as set forth below in the new grounds of rejection.

In response to applicant's argument that "Sastry is not the same nonanalogous art", it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "a sender", "a receiver connected to said IP network for receiving data transmitted over said IP network", "a switch", and the output of said switch connected to said IP network", as taught by Sastry in the system of Zahn, so that it would increase the support for the number of simultaneous calls/real-time data transmission and efficient resource allocation; see Sastry col. 3, line 15-30; see col. 7, line 5-12.

Regarding Claim 2, Zahn discloses wherein the setup and adaptation of the second processing is started using a trigger event (see FIG. 1, PULL request 1 is used to being processing video frames in CPU 5'; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4).

Regarding Claim 3, Zahn discloses wherein the switching is performed after the completion of the setup and/or adaptation of the second processing unit (see FIG. 2, switching/changing to CPU 5' after setup/configuration/setting CPU 5'; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

In response to argument based on Mr. Funaya statements, the combined system of Zahn and Sastry still discloses the broadly claim invention as set detailed below. Also, examiner responses with regards to Mr. Funaya statement in previous action are hereby incorporated.

Regarding claim 5, the applicant argued that, "...Muniere cannot be combined with Zahn to make a workable system. The two are in entirely different technical fields...There is no basis in fact for the conclusion of obviousness..." in page 13-14.

In response to applicant's argument, the examiner respectfully disagrees with the argument above.

In response to applicant's argument that "*the two are in entirely different technical fields*" (i.e. nonanalogous art), it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, the combined system of Zahn, Sastry and Muniere and the applicant's invention are

concerted with the certain switching condition (see FIG. 4, Switch 41) is whether at least one given parameter reaches at a predetermined value (see FIG. 3-4, switching is performed according to meeting threshold/maximum High/low priority data counts; see col. 5, line 4-55; see col. 6, line 26-45). Thus, it is clear that Muniere is the analogous art.

In response to applicant's argument, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this case, Muniere is not bodily incorporated into the combined system of Zahn and Sastry, rather the teaching of Muniere is used to modify the combined system.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, applicant is arguing Zahn and Muniere individually, however, in fact the rejection is based on the combined system of Zahn, Sastry and Muniere, Thus, it is obvious to combine Zahn, Sastry and Muniere.

Regarding claims 1-18, the applicant argued that, "…Ochi has nothing to do with the claims in the present application and it works entirely differently…in contrast, Ochi approach is specifically *not* intended for real-time, low-delay scenarios and relies upon parallel processing components...Ochi apparatus does not anticipated or suggest the disclosed claimed invention…" in pages 15-19.

In response to applicant's argument, the examiner respectfully disagrees with the argument above.

It is noted that applicant broadly argues "*Ochi has nothing to do with the claims in the present application and it works entirely differently*", instead of specifically point out what Ochi allegedly missing. The reason why applicant was **unable** to specifically point out what Ochi allegedly missing is because Ochi discloses every single limitation recited in the broadly claimed invention. The combined of Ochi and Sastry clearly disclose the time-synchronous multi-media data, which is a video data, parallel transmission, apparatus as detailed in rejection below.

Claim Objections

7. Claims 1-18 are objected to because of the following informalities:

Claim 1 recites **"a sender"** in lines 2 and 6. For consistency and clarification, it is suggested to change "a sender" in line 6, to "**the** sender".

Claim 1 recites **"a receiver"** in lines 2 and 9. For consistency and clarification, it is suggested to change "a receiver" in line 9, to "**the** sender".

Claim 1 recites **"a plurality of said multiple subcomponents"** in lines 14 and 19. For consistency and clarification, it is suggested to change "**a plurality of said multiple subcomponents**" in line 14, to "**a plurality of said multiple subcomponents of the first processing unit**" and "**a plurality of said multiple subcomponents of the second processing unit"**, or equivalent thereof.

Claim 1 recites **"the time-synchronous data"** in lines 13 and 18. For consistency and clarification, it is suggested to change "**the time-synchronous multi-media data**" in line 2, to "**the** sender".

Claim 1 recites **"the time-synchronous data"** in lines 13 and 18. For consistency and clarification with "**time-synchronous multi-media data**" in line 2, it is suggested to change "**the time-synchronous data**" in line 13 and 18, to "**the time-synchronous multi-media data**".

Claims 2-18 are also objected since they are depended upon objected claim 1 as set forth above.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 1-4 and 6-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zahn (WO 00/62254) in view of Sastry (US006694373B1).

Regarding Claim 1, Zahn discloses an apparatus (see FIG. 1,2; apparatus 1) for the transmission of time-synchronous multi-media data (see FIG. 3, real time/synchronous video/multi-media signal 50; see page 4, paragraph 3-8; see page 9, last paragraph; real time/synchronous video/multi-media signal utilizing MPEG or HDTV) from a sending means to a receiving means using a network (see page 4-6; a video signal must transmit from a

transmitting/sending means to a customer/receiving means over a network), wherein the time-synchronous data is processed and transmitted at the sender as well as the receiver (see FIG. 1, 2,4,5, the video data is processed at transmitter or receiver/customer; see page 9, last paragraph), comprising:

receiving time-synchronous multi-media data **(see FIG. 1, 2, receiving real time/synchronous video/multi-media signal 50 (see FIG. 3) utilizing MPEG or HDTV at apparatus 1; page 4, paragraph 3-8; see page 9, last paragraph)**;

a mechanism for processing the time-synchronous multi-media data for output to said network **(see FIG. 1-2, apparatus 1 comprises a mechanism for processing real time/synchronous video/multi-media signal 50 (see FIG. 3) utilizing MPEG or HDTV for transmitting/outputting to a network; see page 9, last paragraph to page 10, second paragraph)**;

the time-synchronous multi-media data transmitted over the network (see FIG. 1-2, **real time/synchronous video/multi-media signal 50 (see FIG. 3) utilizing MPEG or HDTV for transmitting/outputting to a network);**

said mechanism comprising:

a first processing unit (see FIG. 1, 2,4,5, a combined system of Processor CPU 5 (for rendering/manipulation by using a modified filter) and memory 6; see page 9, last paragraph; entire page 10) composed of multiple subcomponents (see FIG. 1,2,4,5, CPU 5 (for rendering/manipulation by using a modified filter) and memory 6), each subcomponent being designed to process the time-synchronous data in a specific and different way (see FIG. 1,2,4,5, CPU 5 process the **video/multi-media** signal in specific/particular and different/dissimilar

way/method (e.g. processing of video data signal) from memory 6, and memory 6 process the **video/multi-media** signal in specific/particular and different/dissimilar way/method (e.g. storing the **video/multi-media** data signal) from CPU 5; see page 9, last paragraph),

a plurality of said multiple subcomponents being selected from the group consisting of a filter **(see FIG. 1, 3, rendering/manipulations performed by a CPU 5 includes applying a modified filter, thus CPU 5 includes a modified filter; entire page 10)**;

a second processing unit parallel to the first processing unit (see FIG. 1,2, 4,5, a combined system of Processor CPU 5' (for rendering/manipulation by using a modified filter) and memory 6', where a combined system of CPU 5 and memory 6 is parallel to a combined system of CPU 5' and memory 6'; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2 to page 13, paragraph 2), composed of multiple subcomponents (see FIG. 1,2,4,5, CPU 5' and memory 6'), each subcomponent being designed to process the time-synchronous data in a specific and different way (see FIG. 1,2,4,5, CPU 5' process the video signal in specific/particular and different/dissimilar way/method (e.g. processing of video data signal) from memory 6', and memory 6' process the video signal in specific/particular and different/dissimilar way/method (e.g. storing the video data signal) from CPU 5'; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2 to page 13, paragraph 2);

a plurality of said multiple subcomponents being selected from the group consisting of a filter **(see FIG. 1, 3, rendering/manipulations performed by a CPU 5' includes applying a modified filter, thus CPU 5' includes a modified filter; entire page 10)**;

wherein the subcomponents of second processing unit are setup and adapted based on changed sender data rate or network characteristics (see page 4, paragraph 3-4, page 8, paragraph

3-7; page 11, paragraph 1 to page 12, paragraph 3; see page 13, paragraph 5-6, last paragraph; CPU 5' and memory 6' are setup and fit/adapted for parallel storage and processing according to sender/transmitter/source increasing/changing real time data rate (i.e. data rate 4 or 8 times/factor of 25/30 frames/second that carriers high resolution format), or real time data load or bandwidth/delay (i.e. network characteristic)) by configuring attribute parameters of the subcomponents (see page 4, paragraph 3-4, page 8, paragraph 3-7; page 11, paragraph 1 to page 12, paragraph 3; see page 13, paragraph 5-6, last paragraph; by setting/configuring resolution format and latency/congestion of CPU 5' and storage/capacity/load of memory 6'),

wherein data processing and transmission of the time-synchronous multi-media data is continued within the first processing unit during the setup and adaptation of the second processing unit (see page 11, paragraph 1-3; processing and transmission of real time **video/multi-media** packet (e.g. MPEG packet, or packet 101) is continued/parallel-processed in the CPU 5 while CPU 5' is setup and fit/adapted for parallel processing); and

selecting/switching between the first and second processing units (see FIG. 1, line 2, switching/changing/selecting between CPU 5 and CPU 5'; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5), the processing and transmission of the time-synchronous multi-media data initially being performed by the first processing unit (see FIG. 2, processing and transmission of real time video/multi-media data packet primarily/initially performed by the CPU 5; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2 to page 13, paragraph 2) and after switching (see FIG. 1-3, after switching/changing/selecting), the processing and transmission of the time-synchronous multi-media data is performed using the second processing unit (see FIG. 1-3, processing and

transmission of real time **video/multi-media packet** (e.g. MPEG packet, or continue data packet 102) is processed by CPU 5'; see page 4, paragraph 3-4, 8 page 8, paragraph 3-7; page 11, paragraph 1 to page 12, paragraph 3; see page 13, paragraph 5-6, last paragraph) such that the processing and transmission of the time-synchronous multi-media data is performed within the second processing unit (see FIG. 1-3, the pr processing and transmission of real time **video/multi-media** packet (e.g. MPEG packet, or continue data packet 102) is processed by CPU 5'' see page 4, paragraph 3-4, 8 page 8, paragraph 3-7; page 11, paragraph 1 to page 12, paragraph 3; see page 13, paragraph 5-6, last paragraph), the output after selecting/switching being connected to said network **(see FIG. 1-2, 4-5, the output/transmitting after selecting/switching is connected to a network; see page 12, paragraph 2 to page 13, paragraph 5)**.

Although Zahn discloses "sending means, receiving means, network, changing/selecting/switching between the first processing unit and the second processing units and network, and the output after selecting/switching being connected to said network" as set forth above,

Zahn does not explicitly disclose "a sender", "a receiver connected to said IP network for receiving data transmitted over said IP network", "a switch", and the output of said switch connected to said IP network".

However, it is well known in the art video/multi-media data is transmitted from a transmitter to a receiver over IP network, and the selecting/changing/switching is performed by a switch/selector/changer. In particular, Sastry discloses an apparatus (see FIG. 2, server 220/230/260; see FIG. 3, server 310; see FIG. 4,6; server 405/605) for the transmission of time-

synchronous multi-media data (see FIG. 2, real time voice/multi-media data; see col. 3, line 29-31, 48-51, 62-67) from a sender (see FIG. 2, sending/transmitting client/CPE 241-244/251-254) to a receiver (see FIG. 2, receiving client/CPE 251-254/241-244) using a IP network **(see FIG. 2, using IP network 215; see col. 3, line 35-55),** wherein the data is processed and transmitted at the sender as well as the receiver (see FIG. 2,3,4,6, server 310 process and transmitted to sending client 241-244 as well as the receiving client 251-254; see col. 3, line 32 to col. 4, line 10) the comprising:

a sender receiving time-synchronous multi-media stream **(see FIG. 2, sending/transmitting client/CPE 241-244/251-254 device receives real time voice/multi-media data; see col. 3, line 25-65)**;

a mechanism (see FIG. 2, server 220/230/260; see FIG. 3, server 310; see FIG. 4,6; server 405/605 comprises a server mechanism (see FIG. 3)) connected to said sender for processing the time-synchronous multi-media data for output to said IP network (see FIG. 2, connects **sending/transmitting client/CPE 241-244/251-254 device for processing real time voice/multi-media data for transmit/output to IP network 215; see col. 3, line 28 to col. 4, line 30);**

a receiver connected to said IP network for receiving processed time-synchronous multi-media data transmitted over said IP network **(see FIG. 2**, receiving client/CPE 251-254/241-244 connected to IP network 215 for receiving processed **real time voice/multi-media data transmit/output over IP network 215; see col. 3, line 28 to col. 4, line 30);**

said mechanism comprising:

a first processing unit (see FIG. 4, DSP-S 431, see FIG. 6, DSP-S631, or see FIG. 8, DSP 801/802),

a subcomponent being selected from the group consisting of a codec **(see FIG. 4, DSP-S 431, see FIG. 6, DSP-S631, or see FIG. 8, DSP 801/802, DSP performs the coding and decoding voice data using Adaptive Differential Pulse Code Modulation (ADPCM), per ITU-T G.726; see col. 5, line 3-25; see col. 6, line 55-69)**;

and a second processing unit parallel to the first processing unit (see FIG. 4, 6, 8. DSP-D 439/639/803 parallel to DSP-S 431/631/801),

a subcomponent being selected from the group consisting of a codec **(see FIG. 4, 6, 8. DSP-D 439/639/803 parallel to DSP-S 431/631/801; DSP performs the coding and decoding voice data using Adaptive Differential Pulse Code Modulation (ADPCM), per ITU-T G.726; see col. 5, line 3-25; see col. 6, line 55-69)**;

wherein data processing and transmission of the time-synchronous multi-media data is continued within the first processing unit during the setup and adaptation of the second processing unit (see col. 4, line 32-60; see col. 5, line 12-20; processing and transmission of **real time voice/multi-media data** is continued/process-parallel in the DSP-S 431/631/801 while setting-up/construction and adapting/configuring DSP-D 439/639/803 for parallel processing) and

a switch selecting between the first and second processing units (see FIG. 4,6, switch 420/620), the processing and transmission of the time-synchronous multi-media data initially being performed by the first processing unit (see FIG. 4,6, 8, processing and transmission of real time voice/ multi-media data primarily/initially performed by the DSP-S) and after switching by

the switch (see FIG. 4, 6, 8, after switching by a switch 420/620; see col. 4, line 39-62; see col. 5, line 10-26, 36-56; see col. 6, line 12-20l; see col. 6, line 55 to col. 7, line 11), the processing and transmission of the time-synchronous multi-media data is performed using the second processing unit such that the processing and transmission of the time-synchronous data is performed within the second processing unit (see FIG. 4,6,8, processing and transmission of real time voice/ multi-media data is performed using the DSP-D (or any another DSP besides DSP-S) such that processing and transmission of the real time voice/ multi-media data is performed within DSP-D (or another DSP); see col. 4, line 39-62; see col. 5, line 10-26, 36-56; see col. 6, line 12-20l; see col. 6, line 55 to col. 7, line 11);

the output of said switch being connected to said IP network (**see FIG. 2, 4, the output of the switch 420 after selecting DSP is connected to IP network 215; see col. 3, line 45-69; see col. 4, line 39-62; see col. 5, line 10-26, 36-56; see col. 6, line 12-20l; see col. 6, line 55 to col. 7, line 11**).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "a sender", "a receiver connected to said IP network for receiving data transmitted over said IP network", "a switch", and the output of said switch connected to said IP network", as taught by Sastry in the system of Zahn, so that it would increase the support for the number of simultaneous calls/real-time data transmission and efficient resource allocation; see Sastry col. 3, line 15-30; see col. 7, line 5-12.

Regarding Claim 2, Zahn discloses wherein the setup and adaptation of the second processing is started using a trigger event (see FIG. 1, PULL request 1 is used to being

processing video frames in CPU 5'; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4).

Regarding Claim 3, Zahn discloses wherein the switching is performed after the completion of the setup and/or adaptation of the second processing unit (see FIG. 2, switching/changing to CPU 5' after setup/configuration/setting CPU 5'; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 4, Zahn discloses wherein the switching is performed after reaching a certain switching condition (see FIG. 2, switching/changing to CPU 5' after frame 101 is processed by CPU 5; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 6, Zahn discloses wherein the time-synchronous multi-media data is processed in the first processing unit using a plurality of said multiple subcomponents (see FIG. 2, real time/synchronous **video/multi-media** signal is processed in the first combined processing system comprising CPU 5 and memory 6; see page 12, paragraph 2).

Regarding Claim 7, Zahn discloses wherein the subcomponents includes at least one of a memory buffer (see FIG. 2, a first combined processing system comprising memory 6; see page 12, paragraph 2).

Regarding Claim 8, Zahn discloses wherein the time-synchronous data is processed in the second processing unit using a plurality of subcomponents (see FIG. 2, a second combined processing system comprising CPU 5' and memory 6'; see page 12, paragraph 2).

Regarding Claim 9, Zahn discloses wherein the subcomponents includes at least one of a memory buffer (see FIG. 2, a second combined processing system comprising memory 6'; see page 12, paragraph 2).

Regarding Claim 10, Zahn discloses wherein the subcomponents are connected during the setup (see FIG. 2, CPU 5' and memory 6' are connected during the configuration/setups; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 11, Zahn discloses wherein the first and second processing unit is initialized after the setup (see FIG. 2, a combined system of CPU 5/5' and memory 6/6' initialized/started/begin processing after the configuring/setting-up the each pipeline connections 1; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 12, Zahn discloses wherein each of the subcomponents of the second processing unit is adapted to the other subcomponents (see FIG. 2, CPU 5' and memory 6' of the combined system of CPU 5' and memory 6' is adapted/fit/adjust/corresponds to other CPU 5/5" and memory 6/6"; see page 12, paragraph 2), or the changed data rate, or changed network characteristics (see page 8, paragraph 3-7; page 11, paragraph 1 to page 12, paragraph 3; see page 13, paragraph 5-6; parallel processing accommodate/conform to the network dynamic/change nature of real time data rate or bandwidth/delay (i.e. network characteristics)).

Regarding Claim 13, Zahn discloses wherein after the switching process, the subcomponents of the first processing unit are de-attached from each other (see FIG. 2, after switching/changing to CPU 5', CPU 5 and memory 6 are separated/de-attached from CPU 5' and

memory 6; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 14, Zahn discloses a plurality of the second processing units is setup and after switching by the switch (see FIG. 2, a second combined system of CPU 5' and memory 6' and a third combined system of CPU 5" and memory 6" are configured/setup, and after switching by the switch); and the subcomponents of the first processing unit (see FIG. 2, a first combined processing system comprising CPU 5 and memory 6; see page 12, paragraph 2).

Zahn does not explicitly disclose "subcomponents of the first processing unit are included in one of the second processing units".

However, Sastry discloses a plurality of the second processing units is setup (see FIG. 8, DSP 803,504,805,806 are setup/configured/constructed) and after switching by the switch after switching by the switch, the subcomponents of the first processing unit are included in one of the second processing units (see FIG. 8, after switching by a switch 420/620, subcomponent 2 ADPCM (Adaptive Pulse Code Modulation for voice compressing) from DSP 801 (i.e. first processing unit) are now included in the DSP 803; see col. 6, line 55 to col. 7, line 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made provide "subcomponents of the first processing unit are included in one of the second processing units", as taught by Sastry in the system of Zahn, for the same motivation as set forth above in claim 1.

Regarding Claim 15, Zahn discloses wherein after switching by the switch, the subcomponents of the first processing unit remain connected (see FIG. 2, after

switching/changing to CPU 5', CPU 5 and memory 6 are still connected; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 16, Zahn discloses wherein a plurality of second processing units (see FIG. 2, a combined system of 5" and memory 6", and more pipelines 1) are setup and adapted based on changed data load and network characteristics (see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5; third combined system of 5" and memory 6" or more pipelines are setup/configured to accommodate/conform to the network dynamic/change nature of real time data load or bandwidth/delay (i.e. network characteristics)).

Regarding Claim 17, Zahn discloses wherein an additional processing unit (see FIG. 2, a combined system of CPU 5" and memory 6") for the processing and/or transmission of time-synchronous multi-media data is used in sequence with the first and second processing units (see FIG. 2, a combined system of CPU 5" and memory 6" process the **real time/synchronous video/multi-media signal** data (i.e. processing of frame 103) in parallel sequence with first and second combined systems (i.e. processed frames 101 and 102); see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 18, Zahn discloses wherein the time-synchronous multi-media data is gathered with one of mechanisms for acquiring visual data and speech data (see page 4, paragraph 3-8; see page 9, last paragraph; real time/synchronous video/multi-media signal data is collected/received by a apparatus 1 for obtaining/acquiring video data (i.e. image/visual data and audio/speech data)).

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zahn and Sastry, and further in view of Muniere (US007095717B2).

Regarding Claim 5, Zahn discloses wherein the certain switching condition is whether at least one given parameter (see FIG. 2, switching/changing to CPU 5' or 5" is based on whether frame 101 is processed by CPU 5; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Zahn does not explicitly disclose "reaches at a predetermined value".

However, Muniere teaches the certain switching condition (see FIG. 4, Switch 41) is whether at least one given parameter reaches at a predetermined value (see FIG. 3-4, switching is performed according to meeting threshold/maximum High/low priority data counts; see col. 5, line 4-55; see col. 6, line 26-45).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide switching when "reaching a predetermined value", as taught by Muniere in the combined system of Zahn and Sastry, so that it would provide guaranteeing a minimum time interval for transmission of data packets; see Muniere col. 6, line 40-45.

11. Claims 1-13, 15, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochi (U.S. 5,299,003) in view of Sastry (US006694373B1).

Regarding Claim 1, Ochi discloses an apparatus (see FIG. 1; signal processing apparatus) for the transmission of time-synchronous multi-media data (see FIG. 1, transmission of video/ multi-media signals; see col. 6, line 26-30) from a sending means (see FIG. 1,

sending/transmitting means that connects to input terminal 10) to a receiving means (see FIG. 1, receiving means that connects to output terminal 21) using a network (see FIG. 1; a network that connects between sending/transmitting means, signal processing device, and the receiving means), wherein the time-synchronous multi-media data is processed and transmitted at sending means as well as the receiving means (see FIG. 1, the video/multi-media signal is processed and transmitted at input terminal 10 as well as the output terminal 21; see col. 5, line 55-60; see col. 6, line 20-45), the comprising:

receiving time-synchronous multi-media data **(see FIG. 1, the video/multi-media signal is received at input terminal 10; see col. 5, line 55-60; see col. 6, line 20-45)**;

a mechanism **(see FIG. 1; signal processing apparatus having a video signal processing mechanism)** for processing the time-synchronous multi-media data for output to a network **(processing video/multi-media data signal for transmitting/outputting to a network; see col. 5, line 55 to col. 6, line 45)**;

the time-synchronous multi-media data transmitted over the network (see FIG. 1, **video/multi-media data signal transmitted over the network from output terminal 21; see col. 5, line 55 to col. 6, line 45);**

said mechanism comprising:

a first processing unit (see FIG. 1, a combined system of first memory 12, transmitter 14 and third memory 16) composed of multiple subcomponents (see FIG. 1, first memory 12, transmitter 14 and third memory 16), each subcomponent being designed to process the time-synchronous data in a specific and different way (see FIG. 1, first memory 12 process the video signal in specific/particular and different/dissimilar way/method (e.g. storing video data signal

input from transmitter 11) from third memory 16 and transmitter 14; transmitter 14 process the video signal in specific/particular and different/dissimilar way/method (e.g. transmitting video data signal input from memory 12) from first and third memory 12, 16; third memory 16 process the video signal in specific/particular and different/dissimilar way/method (e.g. storing video data signal input from transmitter 14) from first memory 12 and transmitter 14; see col. 5, line 55 to col. 6, line 55); a plurality of said multiple subcomponents being selected from the group **(see FIG. 1, a plurality of first memory 12, transmitter 14 and third memory 16; see col. 5, line 55 to col. 6, line 55)**;

a second processing unit parallel to the first processing unit (see FIG. 1, a combined system of second memory 13, transmitter 15 and fourth memory 17 is parallel to a combined system of first memory 12, transmitter 14 and third memory 16; see col. 5, line 55 to col. 6, line 55), composed of multiple subcomponents (see FIG. 1, second memory 13, transmitter 15 and fourth memory 17), each subcomponent being designed to process the time-synchronous data in a specific and different way (see FIG. 1, second memory 13 process the video signal in specific/particular and different/dissimilar way/method (e.g. storing another video data signal input from transmitter 11) from fourth memory 17 and transmitter 15; transmitter 15 process the video signal in specific/particular and different/dissimilar way/method (e.g. transmitting video data signal input from memory 13) from second and fourth memory 13,17; fourth memory 17 process the video signal in specific/particular and different/dissimilar way/method (e.g. storing video data signal input from transmitter 15) from second memory 13 and transmitter 15; see col. 5, line 55 to col. 6, line 55); a plurality of said multiple subcomponents being selected from the

group (**see FIG. 1, a plurality of second memory 13, transmitter 15 and fourth memory 17; see col. 5, line 55 to col. 6, line 55**);

wherein the subcomponents of second processing unit are setup and adapted based on changed sender data rate or network characteristics (see FIG. 2a-h, memory 13,17 and transmitter 15 are configured/setup and fit/adapted for parallel storage and processing according to transmitting/sending data rate or network transmission characteristic; see col. 5, line 55 to col. 6, line 55) by configuring attribute parameters of the subcomponents (see col. 5, line 55 to col. 6, line 55; by setting/configuring timing parameters of the memory 13,17 and transmitter 15),

wherein data processing and transmission of the time-synchronous multi-media data is continued within the first processing unit during the setup and adaptation of the second processing unit (see FIG. 1, 2a-h, processing and transmission of video/ multi-media data is continue at t0 to t1, t2 to t3, and t4 to t5 within the combined system of first memory 12, transmitter 14 and third memory 16 during the configuration/setup and fitting/adaptation of a combined system of second memory 13, transmitter 15 and fourth memory 17; see col. 6, line 26 to col. 7, line 10);

a switch (see FIG. 1, Switch circuit 18) selecting between the first and second processing units (see FIG. 1, switching/changing/selecting between the combined system of first memory 12, transmitter 14 and third memory 16, and the combined system of second memory 13, transmitter 15 and fourth memory 17; see col. 6, line 6-55), the processing and transmission of the time-synchronous multi-media data initially being performed by the first processing unit (see FIG. 1, 2a-h, processing and transmission of **video/ multi-media** primarily/initially performed by the combined system of first memory 12, transmitter 14 and third memory 16 at t0 to t1, t2 to

t3, and t4 to t5) and after switching, the processing and transmission of the time-synchronous multi-media data is performed using the second processing unit (see FIG. 1, 2a-h, after switching processing and transmission of **video/ multi-media data** signal is processed by the combined system of second memory 13, transmitter 15 and fourth memory 17 at t1 to t2, t3 to t4, and t5 to t6) such that the processing and transmission of the time-synchronous multi-media data is performed within the second processing unit (see FIG. 1, 2a-h, such that the processing and transmission of **vide/ multi-media** data signal is performed by the combined system of second memory 13, transmitter 15 and fourth memory 17); see col. 6, line 26 to col. 7, line 10),

the output of said switch being connected to said network **(see FIG. 1, the output of switch 18 is connected to the network; see col. 6, line 26 to col. 7, line 10).**

Although Ochi discloses "sending means, receiving means, network, a plurality of said multiple subcomponents" as set forth above,

Ochi does not explicitly disclose "a sender", "a receiver connected to said IP network for receiving data transmitted over said IP network", selected from the group consisting of "a codec".

However, it is well known in the art video/multi-media data is transmitted from a transmitter to a receiver over IP network, and the selecting/changing/switching is performed by a switch/selector/changer. In particular, Sastry discloses an apparatus (see FIG. 2, server 220/230/260; see FIG. 3, server 310; see FIG. 4,6; server 405/605) for the transmission of time-synchronous multi-media data (see FIG. 2, real time voice/multi-media data; see col. 3, line 29-31, 48-51, 62-67) from a sender (see FIG. 2, sending/transmitting client/CPE 241-244/251-254) to a receiver (see FIG. 2, receiving client/CPE 251-254/241-244) using a IP network **(see FIG. 2,**

using IP network 215; see col. 3, line 35-55), wherein the data is processed and transmitted at the sender as well as the receiver (see FIG. 2,3,4,6, server 310 process and transmitted to sending client 241-244 as well as the receiving client 251-254; see col. 3, line 32 to col. 4, line 10) the comprising:

a sender receiving time-synchronous multi-media stream **(see FIG. 2, sending/transmitting client/CPE 241-244/251-254 device receives real time voice/multi-media data; see col. 3, line 25-65)**;

a mechanism (see FIG. 2, server 220/230/260; see FIG. 3, server 310; see FIG. 4,6; server 405/605 comprises a server mechanism (see FIG. 3)) connected to said sender for processing the time-synchronous multi-media data for output to said IP network (see FIG. 2, connects **sending/transmitting client/CPE 241-244/251-254 device for processing real time voice/multi-media data for transmit/output to IP network 215; see col. 3, line 28 to col. 4, line 30);**

a receiver connected to said IP network for receiving processed time-synchronous multi-media data transmitted over said IP network **(see FIG. 2**, receiving client/CPE 251-254/241-244 connected to IP network 215 for receiving processed **real time voice/multi-media data transmit/output over IP network 215; see col. 3, line 28 to col. 4, line 30);**

said mechanism comprising:

a first processing unit (see FIG. 4, DSP-S 431, see FIG. 6, DSP-S631, or see FIG. 8, DSP 801/802),

a subcomponent being selected from the group consisting of a codec **(see FIG. 4, DSP-S 431, see FIG. 6, DSP-S631, or see FIG. 8, DSP 801/802, DSP performs the coding and**

decoding voice data using Adaptive Differential Pulse Code Modulation (ADPCM), per ITU-T G.726; see col. 5, line 3-25; see col. 6, line 55-69);

and a second processing unit parallel to the first processing unit (see FIG. 4, 6, 8. DSP-D 439/639/803 parallel to DSP-S 431/631/801),

a subcomponent being selected from the group consisting of a codec (**see FIG. 4, 6, 8. DSP-D 439/639/803 parallel to DSP-S 431/631/801; DSP performs the coding and decoding voice data using Adaptive Differential Pulse Code Modulation (ADPCM), per ITU-T G.726; see col. 5, line 3-25; see col. 6, line 55-69**);

wherein data processing and transmission of the time-synchronous multi-media data is continued within the first processing unit during the setup and adaptation of the second processing unit (see col. 4, line 32-60; see col. 5, line 12-20; processing and transmission of **real time voice/multi-media data** is continued/process-parallel in the DSP-S 431/631/801 while setting-up/construction and adapting/configuring DSP-D 439/639/803 for parallel processing) and

the output of said switch being connected to said IP network (**see FIG. 2, 4, the output of the switch 420 after selecting DSP is connected to IP network 215; see col. 3, line 45-69; see col. 4, line 39-62; see col. 5, line 10-26, 36-56; see col. 6, line 12-20; see col. 6, line 55 to col. 7, line 11**).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "a sender", "a receiver connected to said IP network for receiving data transmitted over said IP network", selected from the group consisting of "a codec", as taught by Sastry in the system of Ochi, so that it would increase the support for the

number of simultaneous calls/real-time data transmission and efficient resource allocation; see Sastry col. 3, line 15-30; see col. 7, line 5-12.

Regarding Claim 2, Ochi discloses wherein the setup and adaptation of the second processing is started using a trigger event (see FIG. 3a-j, the configuration/setting-up and fitting/adaptation of a combined system of second memory 13, transmitter 15 and fourth memory 17 is began/stated using waveform up/down event; see col. 6, line 26 to col. 7, line 10).

Regarding Claim 3, Ochi discloses wherein the switching is performed after the completion of the setup and/or adaptation of the second processing unit (see FIG. 1, switching is performed after completion/ending of setup/configuration/setting and adaptation/fitting of the combined system of second memory 13, transmitter 15 and fourth memory 17; see col. 6, line 6-55).

Regarding Claim 4, Ochi discloses wherein the switching is performed after reaching a certain switching condition (see FIG. 2, switching is performed after reaching t1, t3, and/or t5 (i.e. condition) which triggers switching; see col. 6, line 6-55).

Regarding Claim 5, Ochi discloses the certain switching condition is whether at least one given parameter reaches at a predetermined value (see FIG. 2, switching condition is whether the time reaching t1, t3, and/or t5; see col. 6, line 6-55)

Regarding Claim 6, Ochi discloses wherein the time-synchronous multi-media data is processed in the first processing unit using a plurality of said multiple subcomponents (see FIG. 1, **video/ multi-media** data is processed in the a combined system comprising first memory 12, transmitter 14 and third memory 16; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 7, Ochi discloses wherein the subcomponents includes at least one of a memory buffer (see FIG. 1, a combined processing system comprising first memory 12 or third memory 16; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 8, Ochi discloses wherein the time-synchronous multi-media data is processed in the second processing unit using a plurality of said multiple subcomponents (see FIG. 1, **a video/ multi-media** data is processed in a combined system of second memory 13, transmitter 15 and fourth memory 17; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 9, Ochi discloses wherein the subcomponents includes at least one of a memory buffer (see FIG. 1, a combined processing system comprising second memory 13 or fourth memory 17; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 10, Ochi discloses wherein the subcomponents are connected during the setup (see FIG. 1, a combined system of second memory 13, transmitter 15 and fourth memory 17 are connected during the configuration/setups; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 11, Ochi discloses wherein the first and second processing unit is initialized after the setup (see FIG. 1, a combined system of first memory 12, transmitter 14 and third memory 16, and a combined system of second memory 13, transmitter 15 and fourth memory 17 are initialized/started/begin processing after the configuring/setting-up; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 12, Ochi discloses wherein each of the subcomponents of the second processing unit is adapted to the other subcomponents (see FIG. 2, each second memory 13, transmitter 15 or fourth memory 17 is adapted/fit/adjust/corresponds to other second memory 13, transmitter 15 or fourth memory 17; or other first memory 12, transmitter 14 and third memory

16; see col. 5, line 55 to col. 6, line 26), or the changed data rate, or changed network characteristics (changing/switching data rate or network transmission characteristic; see col. 5, line 55 to col. 6, line 55).

Regarding Claim 13, Ochi discloses wherein after the switching process, the subcomponents of the first processing unit are de-attached from each other (see FIG. 1, after switching, first memory 12, transmitter 14 and third memory 16 are separated/de-attached from second memory 13, transmitter 15 or fourth memory 17; see col. 5, line 55 to col. 6, line 55).

Regarding Claim 15, Ochi discloses wherein after switching by the switch, the subcomponents of the first processing unit remain connected (see FIG. 1, after switching memory 12, transmitter 14 and third memory 16 are still connected; see col. 5, line 55 to col. 6, line 26).

Regarding Claim 18, Ochi discloses wherein the time-synchronous multi-media data is gathered with one of mechanisms for acquiring visual data and speech data (see FIG. 1; video data is collected/received by a apparatus for obtaining/acquiring video/ **multi-media** data (i.e. image/visual data and audio/speech data); see col. 5, line 55 to col. 6, line 26).

Regarding Claim 14, Ochi discloses the second processing units is setup and after switching by the switch (see FIG. 1, second memory 13, transmitter 15 or fourth memory 17 are configured/setup, and after switching by the switch; see col. 5, line 55 to col. 6, line 55); and the subcomponents of the first processing unit (see FIG. 1, second memory 13, transmitter 15 or fourth memory 17) as set forth above in claim 1.

Ochi does not explicitly disclose "a plurality of the second processing units" and "the subcomponents of the first processing unit are included in one of the second processing units".

Sastry discloses a plurality of the second processing units is setup (see FIG. 8, DSP 803,504,805,806 are setup/configured/constructed) and after switching by the switch after switching by the switch, the subcomponents of the first processing unit are included in one of the second processing units (see FIG. 8, after switching by a switch 420/620, subcomponent 2 ADPCM (Adaptive Pulse Code Modulation for voice compressing) from DSP 801 (i.e. first processing unit) are now included in the DSP 803; see col. 6, line 55 to col. 7, line 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "a plurality of the second processing units" and "the subcomponents of the first processing unit are included in one of the second processing units", as taught by Sastry in the system of Ochi, so that it would increase the support for the number of simultaneous calls/real-time data transmission and efficient resource allocation; see Sastry col. 3, line 15-30; see col. 7, line 5-12.

Regarding Claim 16, Ochi discloses wherein a second processing unit (see FIG. 1, a combined system of second memory 13, transmitter 15 and fourth memory 17 are configured/setup, and after switching by the switch; see col. 5, line 55 to col. 6, line 55) are setup and adapted based on changed data rate and network characteristics (see FIG. 2a-h, setup/configured and fit/adapted for parallel storage and processing according to transmitting/sending data rate and network transmission characteristic; see col. 5, line 55 to col. 6, line 55).

Ochi does not explicitly disclose "a plurality of the second processing units".

Sastry discloses a plurality of the second processing units is setup (see FIG. 8, DSP 803,504,805,806 are setup/configured/constructed; see col. 6, line 55 to col. 7, line 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "a plurality of the second processing units", as taught by Sastry in the system of Ochi, so that it would increase the support for the number of simultaneous calls/real-time data transmission and efficient resource allocation; see Sastry col. 3, line 15-30; see col. 7, line 5-12.

Regarding Claim 17, Ochi discloses the processing and transmission of time-synchronous multi-media data is used in sequence with the first and second processing units (see FIG. 2, a combined system of memory 12, transmitter 14 and memory 16 process the **video/ multi-media** data (i.e. processing of video) in parallel sequence with second combined system memory 13, transmitter 15, memory 17; see col. 5, line 55 to col. 6, line 55).

Ochi does not explicitly disclose "an additional processing unit".

Sastry discloses wherein an additional processing unit (see FIG. 1, DSP-D 439) for the processing and transmission of data is used in sequence with the first and second processing units (see FIG. 2, processing and transmission of data is used in parallel sequence with DSP-S 431 and DSP 432; see col. 6, line 55 to col. 7, line 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "a plurality of the second processing units", as taught by Sastry in the system of Ochi, so that it would increase the support for the number of simultaneous calls/real-time data transmission and efficient resource allocation; see Sastry col. 3, line 15-30; see col. 7, line 5-12.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to IAN N. MOORE whose telephone number is (571)272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Trost can be reached on 571-272-7872. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ian N. Moore
Primary Examiner
Art Unit 2616

/Ian N. Moore/
Primary Examiner, Art Unit 2616